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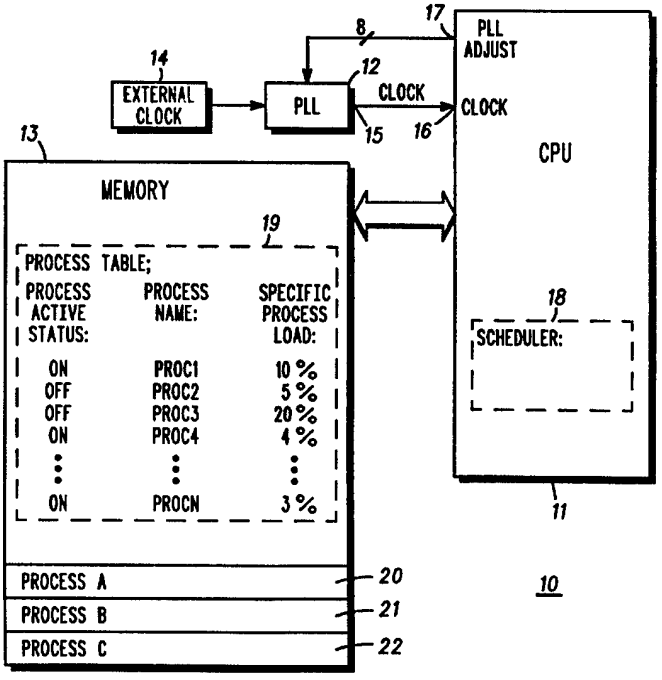
(54) Title: METHOD TO CONTROL A COMPUTER HAVING AN ADJUSTABLE CLOCK GENERATOR AND A MICROPROCESSOR SYSTEM

(57) Abstract

A microprocessor system has a clock (14, 12) for generating a variable clock frequency. There is a process table (19) containing information of processes of the microprocessor system where the information of each process comprises a specific process load information. A clock frequency is calculated from the specific process load information of the processes called and stopped. The clock is controlled to generate a clock frequency corresponding to the calculated clock frequency, thereby reducing the power drain requirement to a minimum value required for the processes called.



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METHOD TO CONTROL A COMPUTER HAVING AN ADJUSTABLE CLOCK GENERATOR AND A MICROPROCESSOR SYSTEM

Field of the Invention

The present invention relates to a computer system having an adjustable clock generator and to a method to control such a computer system.

Background of the Invention

The clock frequency in common microprocessor designs is a fixed value determined by the maximum CPU load. The CPU load over time varies in typical applications and it is only during times of high CPU load the maximum clock frequency is necessary. At other times, the high clock frequency consumes an unnecessary amount of power.

In the prior art, GB2246455 shows a microprocessor to which the clock frequency is chosen by a switch. The control of the switch is activated by a hardware interrupt. A problem with this design is that after the interrupt has occurred the clock frequency is fixed, independently of the needed CPU load of the interrupt routine.

Summary of the Invention

According to the invention a method to control a computer having an adjustable clock generator is provided comprising the steps of: providing a process table in memory, said table including respective process load information corresponding to respective processes; and placing the computer in an operational controlling mode which comprises the steps of: selecting at least one process for operation; and calculating a clock frequency from the process load information for the at least one selected process in the process table; and controlling the adjustable clock generator to correspond to the calculated clock frequency.

In this manner, the clock frequency and hence the power drain of the computer is reduced to a minimum value required for the processes called at a given time. Great flexibility is possible in adapting the clock frequency to the processing load at any given time.

A preferred embodiment of the invention will now be described, by way of example only, with reference to the accompanying drawings.

Brief Description of the Drawings

Fig. 1 shows a microprocessor system according to an embodiment of the invention.

Fig. 2 shows a phase locked loop for a microprocessor system according to an embodiment of the invention.

Detailed Description of the Preferred Embodiment

In Fig. 1, a microprocessor system 10 is shown. The microprocessor system comprises central processing unit (CPU) 11, which may, for example, be a Motorola 68040. The system also comprises a phase lock loop (PLL) 12, memory 13 (including at least read only memory) and an external clock 14. The external clock 14 provides a clock signal to the PLL 12, which in turn provides a controlled clock signal 15 to a clock input 16 of the CPU 11. The CPU 11 has a PLL adjust output 17 comprising four data line fed to a controllable counter in the PLL 12. This signal allows the frequency of the output 15 of the PLL to be synthesised according to the status of the PLL adjust signal 17. The CPU 11 additionally has memory 18 including a scheduler.

The memory 13 includes process code of processes to be operated by the CPU and also includes a process table 19 having memory locations for storing the on/off status of a particular process, the process name of that process and a specified process load factor described below. The processes themselves are stored in memory 13 and illustrated as being located at memory locations 20, 21 and 22 etc.

In the illustration, the scheduler is stored in the CPU 11 and the processes and the process table are stored in memory 13, but it should be understood that the physical memory locations of these various elements are irrelevant.

The operation of the microprocessor system is separated in processes A, B and C stored at locations 20, 21 and 22. These processes can be queued up and run sequentially, one at a time, from start to end, or the processes may be identified as tasks in a multi-task operational mode where each task only occupies the CPU for a short period of time. In both cases, the scheduler 18 controls which process or task is to be run. The scheduler

may be part of the operating system of the computer. To enable the scheduler to keep track of the processes, these are listed in the process table 19 stored in the memory 13. Each process is identified by the process name, which could, for example, be the start address to the process or the address from where the process is to continue next time it is run. For each process, a process active status is stored. This status indicates whether the process is active and should be run next time the scheduler allocates time for the process (shown as 'on' in Fig. 1) or if the process is inactive and should not be run (shown as 'off' in Fig. 1). This status information may be changed by the scheduler or by any process.

The CPU load over time varies in typical applications from very low loads, for example 5% load when waiting for an event, to very high loads, for example 95% load when computing a complex algorithm. The same applies for processes. The needed CPU load may differ from one process to another and is dependent on the task or the process.

Each process is allocated a specific process load, illustrated in the right-hand column in process table 19, which corresponds to an anticipated load of the process. For example, the anticipated load may be expressed as a factor which indicates a predetermined load, not dependent on the actual running conditions. The specific process load for each process is stored in the process table 19.

The CPU is repetitively placed in an operational controlling mode, which gives a corresponding command to the scheduler 18. The scheduler selects one of the processes listed as active in the process table 19. Before the selected process is called the scheduler calculates the clock frequency from the specific process load of the selected process. The scheduler commands the PLL circuit 12 by the aid of the PLL adjust status to generate a clock frequency corresponding to the calculated clock frequency.

In the example described above a single process is called up by the scheduler 18 and that process determines the selected CPU clock frequency. Thus, a very demanding process causes the selection of a high clock frequency whereas a less demanding process selects a lower clock frequency, thereby reducing the power drain requirement on the power source (not shown). Whether a process is demanding or less demanding depends on many factors, for example on predetermined rate of processing of data or upon predetermined time of requirement of data output. The specific process load programmed in the process table 19 is pre-selected to take into account these factors.

As an alternative example to the example of running individual processes, two or more processes may run simultaneously. In these circumstances, the clock frequency may be determined by the maximum load factor for all the active processes. Alternatively, it may be determined by the sum of the load factors of the various processes. The choice of these and other alternatives depends upon the nature of interaction of the various processes.

Referring to Fig. 2, details of the PLL circuit 12 are shown. The circuit comprises an external clock input 30, a divider 31, a phase comparator 32, a filter 33, a voltage controlled oscillator (VCO 34), a second divider 35 and a third divider 36. The first divider 31 has a control input 40 and the second divider 36 has a control input 41. In operation, the first divider 31 receives the external clock signal from clock 14 and forms a coarse division depending upon a division factor received on input 40 (which is a four-bit wide input). The resulting divided signal is compared in phase comparator 32 with the output of third divider 36. The phase comparison is filtered in filter 33 and control VCO 34 to provide a variable clock signal on output 15. This clock signal is divided by four in second divider 35 and divided again in adjustable divider 36, which also receives a four-bit wide control signal from CPU 11. It will be appreciated that the output 15 has a frequency which is a multiple of the output from divider 31, that multiple being equal to the multiple of division factors of divider circuits 35 and 36.

The necessary performance of the CPU is adapted to the current load dynamically. The clock frequency and, by that the CPU performance, is reduced to a value that matches the CPU load. The reduction of the clock frequency reduces the power consumption of the system.

It should be understood that the PLL circuit 12 and/or the memory 13 shown in Fig. 1 may be integrated together with the CPU 11.

Thus, it has been described how the processes stored in memory locations 20, 21 and 22, which are called up in an operation mode (phase) of the CPU 11, are called and stopped depending on a status information item present for each process in the process table 19. The process load information of only the call process for one of the call processes is used to calculated the clock frequency while process load information for processes not called is not used to calculate the clock frequency.

While not shown in the process table 19 in Fig. 1, the information corresponding to each process in the process table comprises a start address for the process, identifying the start of the relevant memory

location 20, 21 or 22. The table includes (as shown) process active status information, that is to say at least and on/off status indicator. When the scheduler 18 calls a process, The CPU 13 causes the process active status in the table to change from off to on and when the scheduler 18 stops the process the CPU 11 causes the process active status to change from on to off.

In the case of a base station controller having no cooling fan, with a 45 W transmitter located in the same housing, a reduction in CPU temperature from 100° to 90°C was achieved using an arrangement in accordance with the present invention.

CLAIMS

1. A method to control a computer having an adjustable clock generator (12) comprising the steps of:

providing a process table (19) in memory, said table including respective process load information corresponding to respective processes; and

placing the computer (11) in an operational controlling phase which comprises the steps of:

selecting at least one process for operation (A, B, C); and

calculating a clock frequency from the process load information for the at least one selected process in the process table; and

controlling the adjustable clock generator (12) to correspond to the calculated clock frequency.

2. A method to control a computer according to claim 1 wherein in the operational controlling phase processes are called and stopped depending on an active status information present for each process in the process table and the process load information of only the called processes is used to calculate the clock frequency.

3. A method to control a computer according to claim 1 wherein the processes of the process table are tasks of a multi-task system.

4. A method to control a computer according to claim 1 wherein the adjustable clock generator (12) is a phase locked loop comprising at least one controllable counter (31, 36) to adjust the output frequency of the phase locked loop.

5. A microprocessor system comprising:

a microprocessor (11) having a clock input (16); and

a clock (14, 12) for generating a variable clock frequency, said clock having an output (15) connected to the clock input of the microprocessor; and

means (13) to hold a process table (19) containing information of processes of the microprocessor system where the information of each process comprises a specific process load information; and

means (18) to call and stop processes; and

means (11) to calculate a clock frequency from the specific process load information of the processes called and stopped; and

means (17) to control the clock to generate a clock frequency corresponding to the calculated clock frequency.

6. A microprocessor system according to claim 5 wherein the information corresponding to each process in the process table comprises:

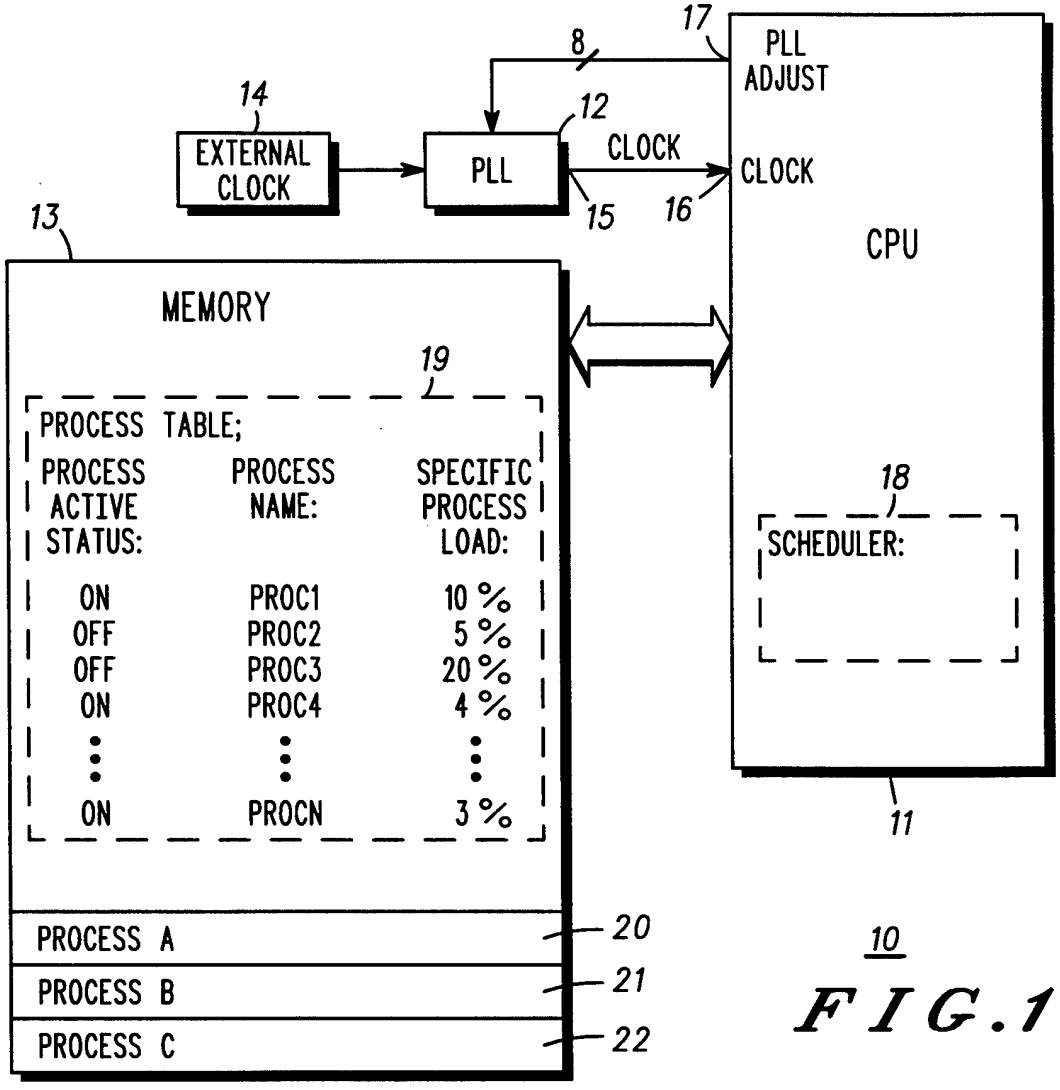
a start address of the process; and

a process active status information.

7. A microprocessor system according to claim 6 wherein the means to call and stop processes comprises means to alter the active status information in the process table.

8. A microprocessor system according to claim 5, wherein the means to generate the clock frequency is a phase locked loop (12) comprising at least one controllable counter (31, 36) to adjust the output frequency of the phase locked loop.

9. A microprocessor system according to claim 5 wherein the process load information comprises a predetermined load factor for each process and the clock frequency is calculated based upon the sum of process load factors for all active processes.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8
PLL
ADJUST
14
12
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CLOCK
PLL
CLOCK
CLOCK
15
16
CPU
13
MEMORY
19
PROCESS TABLE;
PROCESS ACTIVE STATUS:
PROCESS NAME:
SPECIFIC PROCESS LOAD:
ON PROC1 10 %
OFF PROC2 5 %
OFF PROC3 20 %
ON PROC4 4 %
ON PROCN 3 %
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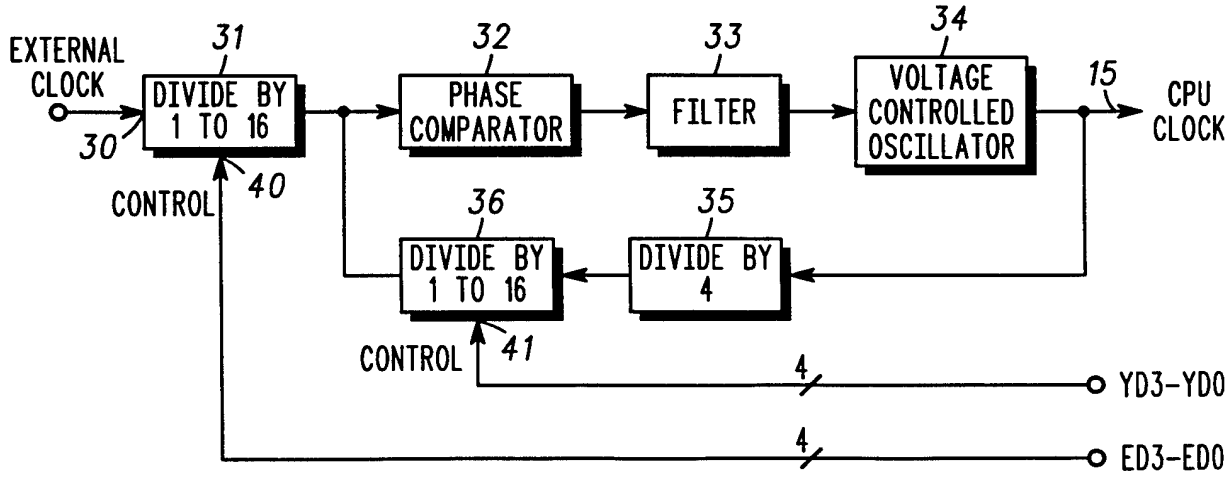
SCHEDULER:
11
PROCESS A
PROCESS B
PROCESS C
20
21
22
10

FIG.1

FIG.2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CONTROL
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PHASE COMPARATOR
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FILTER
34
VOLTAGE CONTROLLED OSCILLATOR
15
CPU CLOCK
36
DIVIDE BY 1 TO 16
CONTROL
41
35
DIVIDE BY 4
4
YD3-YD0
4
ED3-ED0

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/EP 95/00517

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F1/32 G06F1/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MOTOROLA TECHNICAL DEVELOPMENTS, vol. 15, May 1992 SCHAUMBURG, ILLINOIS US, pages 43-44, XP 000306138 YOUNG R. ET AL 'ADAPTIVE CLOCK SPEED CONTROL FOR VARIABLE PROCESSOR LOADING' see the whole document	1-3,5,9
Y	---	4,6-8
X	WO,A,86 00432 (AMERICAN TELEPHONE AND TELEGRAPH COMPANY) 16 January 1986 see page 4, line 26 - page 5, line 25	1,2,5,9
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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
1 June 1995	12. 06. 95

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 15 no. 503 (P-1290) [19] ,19 December 1991 & JP,A,03 217916 (OKI ELECTRIC IND CO) 25 September 1991, see abstract	1,5
Y	EP,A,0 278 140 (HEWLETT PACKARD) 17 August 1988 see column 1, line 25 - line 33; figures 1,2	4,8
Y	THE DESIGN OF OS/2, 1992 page 112,122 DEITEL H. M. AND KOGAN M. S. see page 112, line 15 - line 23 see figure 5.5	6,7
A	EP,A,0 367 369 (OWENS ILLINOIS CLOSURE INC) 9 May 1990 see column 1, line 44 - line 54 see column 4, line 47 - column 6, line 10	6,7

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte. onal Application No
PCT/EP 95/00517

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
WO-A-8600432	16-01-86	US-A-	4670837	02-06-87
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EP-A-278140	17-08-88	JP-A-	63219225	12-09-88
		US-A-	4835491	30-05-89
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		JP-C-	1878304	07-10-94
		JP-A-	2057570	27-02-90
		JP-B-	6000549	05-01-94

DERWENT-ACC-NO: 1995-311636

DERWENT-WEEK: 199541

TITLE: Control method for computer with adjustable clock generator involves calculating clock frequency from specific process load information of process being called and stopped with controlled clock to generate clock frequency corresponding to calculated value

INVENTOR: MEIER W; ROTTGER N

PATENT-ASSIGNEE: MOTOROLA GMBH[MOTI]

PRIORITY-DATA: 1994GB-003633 (February 25, 1994)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE
WO 9523370 A1	August 31, 1995	EN
GB 2287555 A	September 20, 1995	EN

DESIGNATED-STATES: CN US AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE

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WO1995023370A1	N/A	1995WO-EP00517	February 13, 1995
GB 2287555A	N/A	1994GB-003633	February 25, 1994

INT-CL-CURRENT:

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CIPS	G06F1/32 20060101
CIPS	H03L7/183 20060101

ABSTRACTED-PUB-NO: WO 9523370 A1

BASIC-ABSTRACT:

The method involves providing a process table (19) in memory. The table includes respective process load information corresponding to respective processes. A computer (11) is placed in an operational controlling phase to select at least one process (A,B,C) for operation. The computer also calculates a clock frequency from the process load information for the selected process in the process table. Finally an adjustable clock generator (12) in the computer is controlled to correspond to the calculated clock frequency.

The operational controlling phase processes are called and stopped depending on an active status information present for each process in the process table. The process load information of only the called processes is used to calculate the clock frequency.

ADVANTAGE - Reduces power drain requirement to minimum value required for called processes. Greater flexibility due to adaptation of clock frequency to processing load.

CHOSEN-DRAWING: Dwg.1/2

TITLE-TERMS: CONTROL METHOD COMPUTER ADJUST CLOCK GENERATOR CALCULATE FREQUENCY SPECIFIC PROCESS LOAD INFORMATION CALL STOP GENERATE CORRESPOND VALUE

DERWENT-CLASS: T01

EPI-CODES: T01-K; T01-L01;